AVR254/255/354/355 BLOCK DIAGRAM

ALL version
has TUNER module.

TUNER MODULE

TO FUNCTION SEL

TUNER L/R

TUNER CONT

A-BUS OUT
AVR355 OPTION

MULTI_OUT
AVR354&355 OPTION

2CH VOL

NJW1159

6dB AMP

MULTI_MUTE * 2EA

6/8 CHANNEL INPUT

FL/R

SL/R

SBL/R

CEN/SUB

LT

RT

ATT

TONE

PRE-OUT

PRE AMP

FRONT L

FRONT R

SURR L

SURR R

CEN

SUBWOOFER

SBL/MULTI L

SBR/MULTI R

DATA

CLOCK

NJW1197FC2

ANALOG AUDIO

ANALOG 5 IN

ANALOG 4 IN

ANALOG 4 OUT

ANALOG 3 IN

ANALOG 2 IN

ANALOG 2 OUT

ANALOG 1 IN

ANALOG FRONT IN

XM IN

USA VER. ONLY

iPod IN

STEREO or iPod IN

MAIN AMP

HP_AMP

+8dB

MIC SIG

MIC_AMP

+40dB

HP_IN

+12V

H_PHONE OUT
or MIC_INPUT

P-AMP
+29dB

FRONT L

FRONT R

SBL/MULTI L

SBR/MULTI R

SURR L

SURR R

CEN

FL

FR

SBL/ZONE2 LEFT

SBR/ZONE2 RIGHT

SL

SR

CEN

Temp. Sensor

DC/OVER CURRENT

SENS

POWER AMP MUTE

TEMP I/F

HEAT2

PROTECT

P_LINE_FAIL

TO XM PART
(TO VIDEO PART)
+5.3V

REGULATOR
(+5V)

TO TORINO PART
+5V
+1.8V

REGULATOR
(+5V)
(+1.8V)

+9VDH
+9VDH

REGULATOR
(+9V)
(+1.8V)

TO DSP PART
+5VD

TO VIDEO PART
+5V

REGULATOR
(+5V)

+12V

REGULATOR
(+12V)

TO VIDEO PART
(TO IPOD PART)
+9V

TO DSP PART
+15V

REGULATOR
(+9V)

TO VIDEO PART
-9V

-15V

REGULATOR
(-5V)

TO A-BUS PART
+24V

REGULATOR
(+24V)

+VCC1

-VCC1

+VCC2

-VCC2

UNBAL DETECT

+5VL

+5VL REG

P-DOWN

PWR DOWN

+12V

POWER S/W

SUB TRANS

STANDBY

AC OUTLET

AC IN

+VSK

FL

FL

XM_RADIO MODULE

D-

D+

XM_DAT

XM_LRCK

XM_BICK

XM_MCK

XM_DT

AMOUNT 2CH DAC

XM_L

XM_R

USA VER. ONLY

THE BRIDGE II
(iPod)

iPod L/R

iPod TX

iPod RX

TMP86F409NG
(8BIT u-COM for iPod)

iPod IN

iPod CONT

iPod CVBS

iPod CVBS

AVR354 & 355 OPTION

HDMI_IN1

HDMI_IN2

HDMI_IN3

HDMI_OUT

HDMI MCLK

HDMI SCLK

HDMI LRCK

HDMI SD

SII9185
(SW IC)

SII9134
(HDMI TX)

SII9135
(HDMI RX)

I2C & GPIO CONTROL

I2S/DSP_SPDIF

I2S

I2S

HDMI_SPDIF

FLI30336
TORINO
(SCALER)

ST232CDR

RS232C

SDRAM
32M

DDR SDRAM
256M * 2EA

DIGITAL VIDEO
MAX : 1080p

ADV7342
(DAC)

NJM2566
6dB

CONTROL BY I2C

6CH VIDEO OUT

CVBS_TORINO IN
S-VID Y_TORINO IN
S-VID C_TORINO IN
Y1/2/3_ TORINO IN
Cb1/2/3_ TORINO IN
Cr1/2/3_ TORINO IN

CVBS_OUT
S-VID Y_OUT
S-VID C_OUT
Y_OUT
Cb_OUT
Cr_OUT

COAX&OPT. FRONT

OPT.1

OPT.2

OPT.3

COAX.1

COAX.2

COAX OUT

A-BUS IR IN

CARR. OUT

ZONE2 IN

REMOTE IN

REMOTE OUT

D_FL

D_FR

D_SL

D_SR

D_CNT

D_SW

D_SBL

D_SBR

CS42528
A/D, D/A CONVERTER WITH DIR

24.576MHz

XIN

XOUT

AINR

AINL

DIN

DOUT

DIR CONT

MCLK

RST

SDIN1

SDIN2

SDIN3

SDIN4

SCLK1

LRCK1

HDMI SCLK

HDMI LRCK

HDMI SD

CS497004
DSP

CLKIN

XMCK

CMPDAT

CMPCLK

CMPREQ

DAOMCLK

RDATA

RBCK

RLRCK

OMCK

ADDRESS&DATA

SPI Serial Flash
8 Mbit

M12L16161A
16M SDRAM

DSP MCLK

HDMI MCLK

DIR MCLK

HDMI MCLK

74VHC157
2CH MUX

MIR CONT

DSP CONT

FUNC_SW CONT

VOL CONT

MUTE CONT

PH DET

TUNER CONT

RDS CONT

XM CONT

TOSHIBA
16BIT u-COM

REMOTE IN

CARR. OUT

MULTI_IR IN

A-BUS_IR OUT

EEPROM (32 Kbit)

RST IC

POWER AMP CONT

iPod Buffer IC CONT

VIDEO SWITCHING CONT

** EEP_ROM **
FOR BACK-UP MEMORY.

I/PD CONTROL

KEY

VR_ENC.

REMOTE ENC.

STANDBY

POWER DOWN

ST232CDR

RS232C

REMOTE SENSOR

FL DISPLAY

ROTARY ENCODER (MASTER VR)

STANDBY /MODE BLUE

MOMS SWITCH

KEY MATRIX

KEY0~2

VR ENC

(BLUE)
VOLUME Indicator

COMPOSITE 3 IN

COMPOSITE 2 IN

COMPOSITE 2 OUT

COMPOSITE 1 IN

AVR354 & 355 OPTION

THE BRIDGE II IN
(iPod CVBS)

FROM THE BRIDGE II
(iPod)

COMPOSITE FRONT IN

FROM FRONT

FRONT VIDEO

V3

V2

V1

CONT

+6dB

DRV

CVBS

FLI30336 ANALOG INPUT

NJM2595

S-VIDEO FRONT IN

FROM FRONT

S-VID Y

S-VID C

S-VIDEO 3 IN

S-VIDEO 2 IN

S-VIDEO 2 OUT

S-VIDEO 1 IN

NJM2566 ANALOG OUTPUT

COMPOSITE MONITOR OUT

S-VIDEO MONITOR OUT

VIDEO SWITCHING CONTROL BY MCU

FLI30336 ANALOG INPUT

Y1

Y2

Cb1

Cb2

Cr1

Cr2

Y3

Cb3

Cr3

COMPO INPUT1

COMPO INPUT2

COMPO INPUT3

AVR354 & 355 OPTION

NJM2566 ANALOG OUTPUT

COMP_Y_OUTPUT

COMP_Cb_OUTPUT

COMP_Cr_OUTPUT

COMPONENT MONITOR OUT

COMMUNICATION BETWEEN TORINO & TOSHIBA MCU
UART RX/TX

COAX FRONT

OPT FRONT

S-VIDEO FRONT

COMPOSITE FRONT

ANALOG FRONT

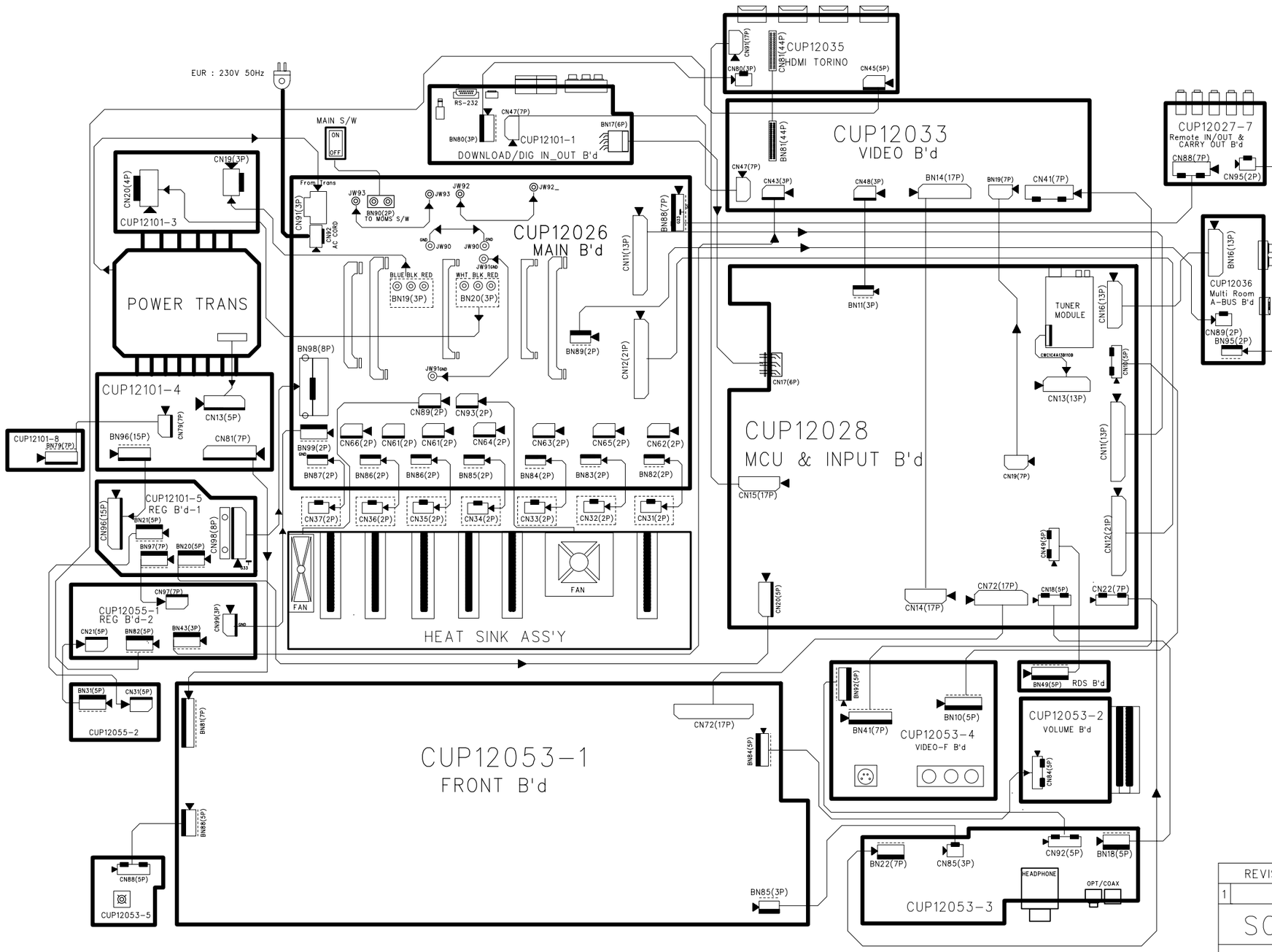
REVISION							
1		2		3		4	
5		6		7			

SCHEMATIC DIAGRAM — SHEET 1/1

MODEL: AVR254/255/354/355

DRAWING NO: BLOCK DIAGRAM 2024BLDZ 1/1

AVR355/230 WIRING DIAGRAM



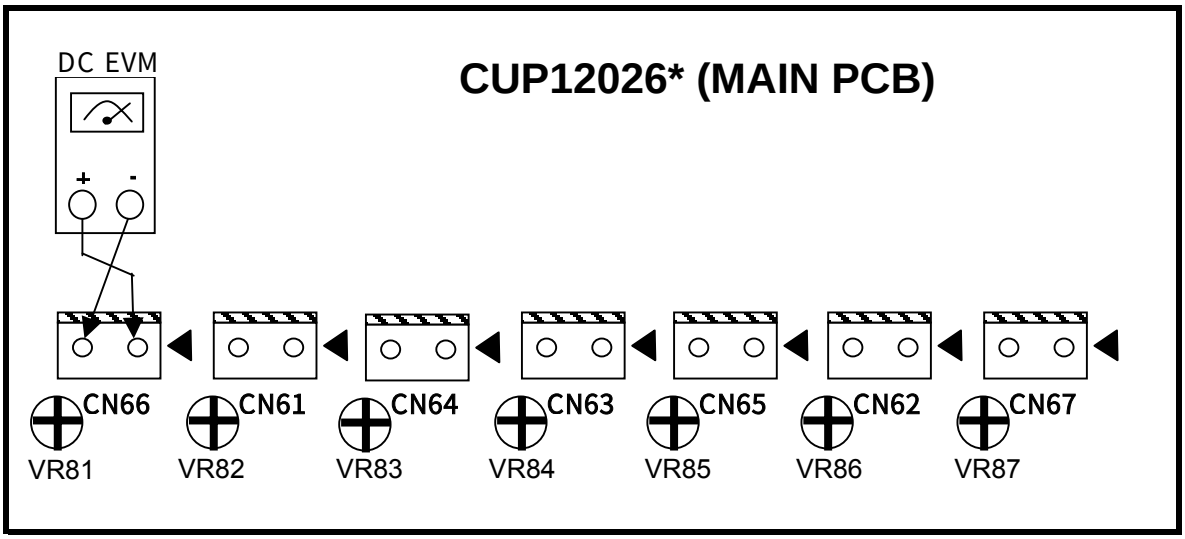
REVISION	2	4	6
1	3	5	7

SCHEMATIC DIAGRAM			SHEET
MODEL	AVR355/230		1/1
DESIGN	CHECK	APPROVE	DRAWING NO
J.T.B	W.Y.Y	K	WIRING DIAGRAM
08.03.11	08.03.11	'3.11	1190SCDZ 1/1

AMPLIFIER SECTION BIAS ADJUSTMENT

Measurement condition
.No input signal or volume position is minimum.

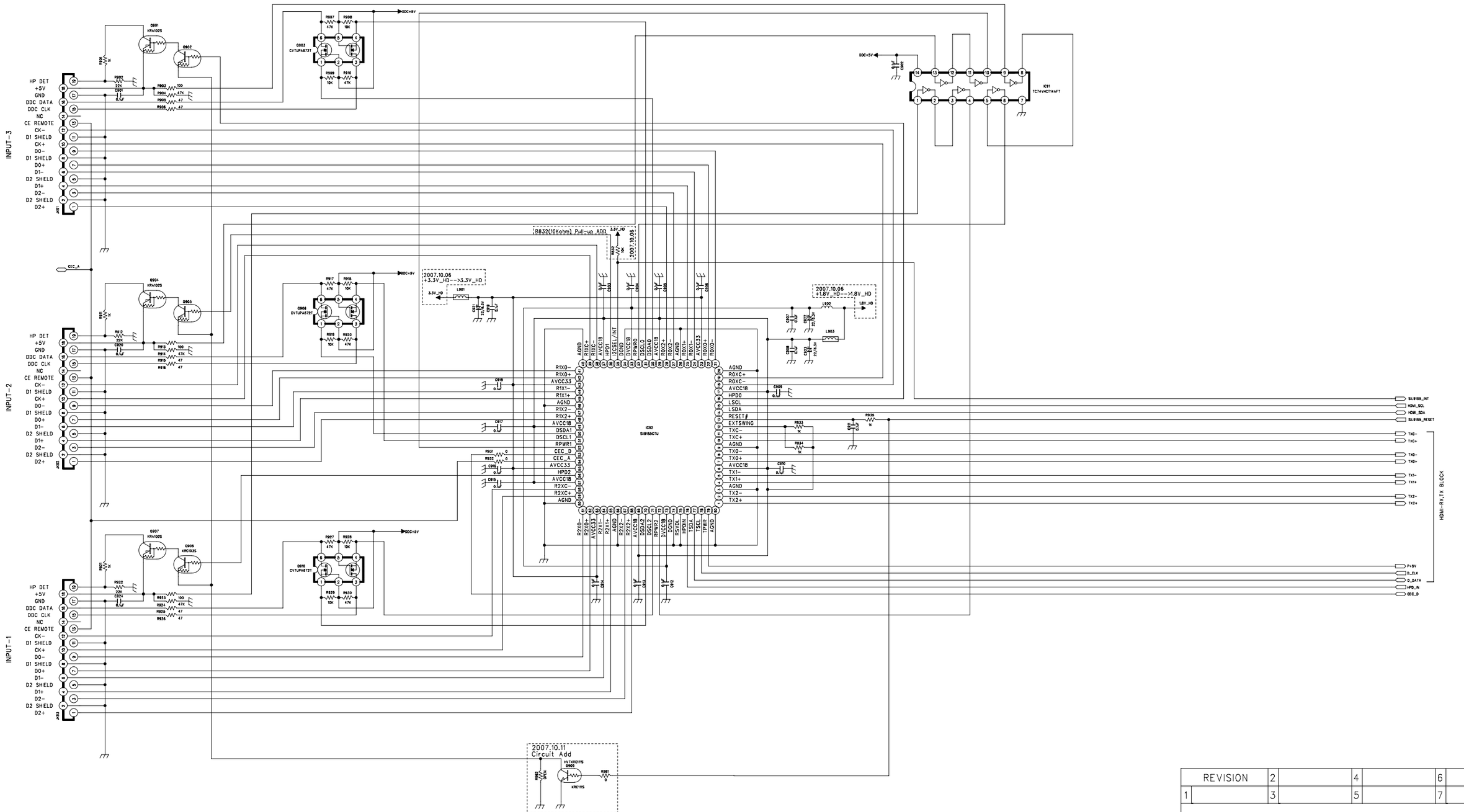
Standard value
.Ideal current = 48mA (± 5%)
.Ideal DC Voltage = 25.92mV (± 5%)



DC VOLTMETER ; Connect to
CN66(SL),CN61(CEN),CN64(SR),CN63(FL),CN65(SBL(AVR254,255,354,355)),CN62(FR),CN67(SBR)

NO.	Channel	Adjust for	Adjustment
1	Front Left	25.92mV (± 5%)	CN63
2	Front Right	25.92mV (± 5%)	CN62
3	Center	25.92mV (± 5%)	CN61
4	Surround Left	25.92mV (± 5%)	CN66
5	Surround Right	25.92mV (± 5%)	CN64
6	Surround Back Left	25.92mV (± 5%)	CN65
7	Surround Back Right	25.92mV (± 5%)	CN67

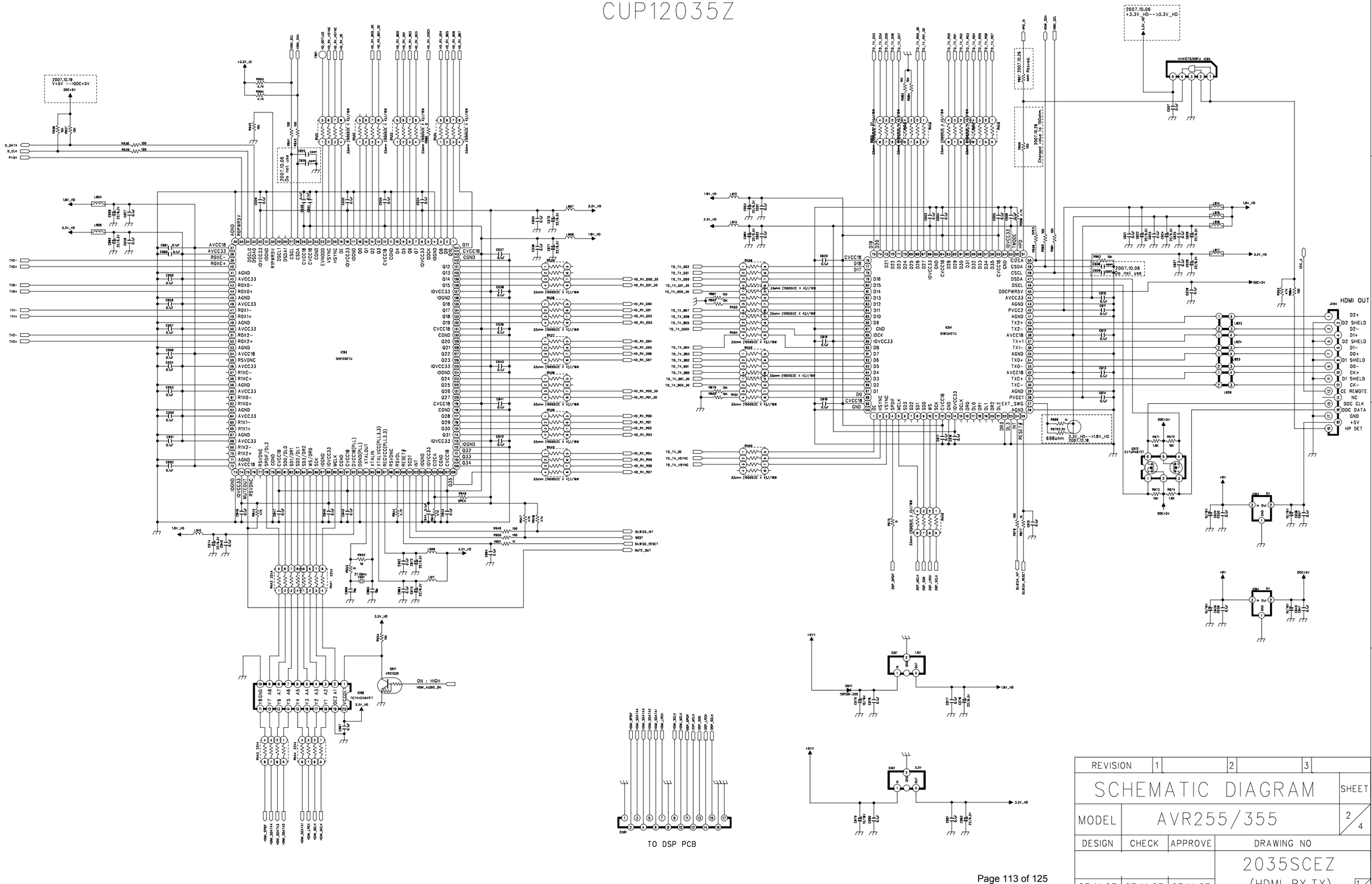
CUP12035Z



REVISION	2		4		6	
1		3		5		7

SCHEMATIC DIAGRAM				SHEET
MODEL	AVR255/355			1/4
DESIGN	CHECK	APPROVE	DRAWING NO	
			2035SCEZ (HDMI-INPUT)	1/1
07.14.07	07.14.07	07.14.07		

CUP12035Z



Page 113 of 125

REVISION	1	2	3	
SCHEMATIC DIAGRAM				SHEET
MODEL	AVR255/355			2/4
DESIGN	CHECK	APPROVE	DRAWING NO	
			2035SCEZ (HDMI-RX,TX)	1/1
07.14.07	07.14.07	07.14.07		

CUP12035Z

ANALOG VIDEO INPUT PORT

COMPONENT IN : 3EA
COMPOSITE IN : 1EA
S_VIDEO IN : 1EA

RGB 10BIT INPUT

B 8BIT INPUT
G 8BIT INPUT
R 8BIT INPUT

*OPTION(Do not use)

*GPROBE

*COMMUNICATION WITH MCU
*CONTROL ROM/VIDEO ENCODER

*IR_IN/NO USE

*EEPROM

*Add 08.01.16 Reserved GPIOs.

2007.10.06 Connect pin3 to CHGND

*DDR MEMORY INTERFACE

*FLASH MEMORY INTERFACE

B 8BIT OUTPUT
G 8BIT OUTPUT
R 8BIT OUTPUT
TTL OUTPUT

RGB 10BIT OUTPUT
TTL OUTPUT

* Need to change 2A

REVISION	2		4		6	
1		3		5		7	

SCHEMATIC DIAGRAM — SHEET 3/4

MODEL: AVR 255/355

DESIGN	CHECK	APPROVE	DRAWING NO
			2035SCEZ (TORINO) 1/1
07.14.07	07.14.07	07.14.07	

CUP12035Z

DO NOT MOVE.

FLI30336
ANALOG INPUT

ADV7342
ANALOG OUTPUT

TO MCU

*OPTION(Do not use)

#VIDEO ENCORDER PART

44	DAC A	Y
43	DAC B	Pb
42	DAC C	Pr
39	DAC D	CVBS
38	DAC E	S-Y
37	DAC F	S-C

R854: 3.9kohm---->6.8kohm
R855: 6.8kohm---->4.3kohm
2007.11.03

Red DATA Input

Blue DATA Input

Green DATA Input

CLOCK DOUBLER(13.5MHz * 2 = 27MHz)

	CLK1
S1:HIGH	iCLK
S1:LOW	2*iCLK

#DDR SDRAM *2EA

DRAWING NO

#FLASH MEMORY

Page 115 of 125

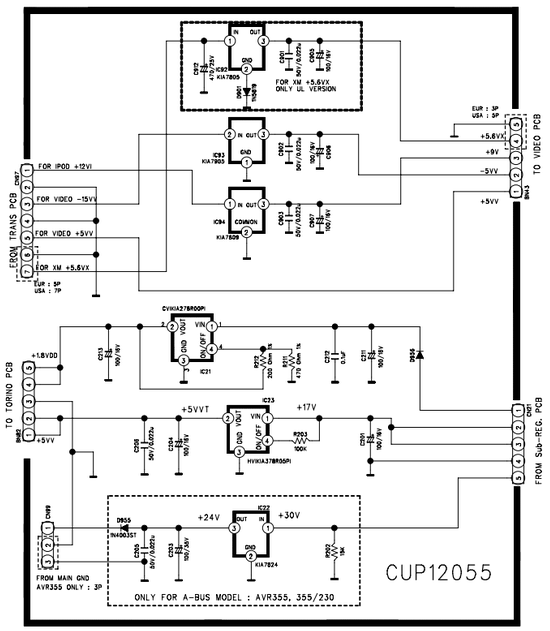
REVISION	2	4	6	
1	3	5	7	

SCHEMATIC DIAGRAM — SHEET 1/4

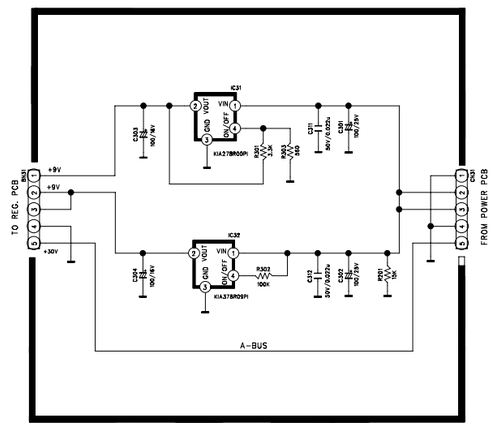
MODEL	AVR255/355

DESIGN	CHECK	APPROVE	DRAWING NO
07.14.07	07.14.07	07.14.07	2035SCEZ (ADV7342+MEM.) 1/1

< REGULATOR PCB >



< Sub-REGULATOR PCB >



LPP

REVISION	2		4		6	
1		3		5		7	

SCHEMATIC DIAGRAM			SHEET
MODEL	AVR 254/255/354/355		1/1
DESIGN	CHECK	APPROVE	DRAWING NO
			CUP12055Z (REGULATOR) 1/1

R201 ~ R216 : 470ohm --> 100ohm
R219 ~ R223 : 470ohm --> 100ohm
R225 ~ R226 : 470ohm --> 100ohm

CD
TAPE R/O P/B
VIDEO3
VIDEO2
VIDEO1 R/O P/B
DVD
8CH Lch
8CH Rch
8CH SLch
8CH SRch
8CH Cch
8CH SUB
8CH SBL
8CH SBR

MIC SIGNAL
VIDEO4-R
VIDEO4-L
From FRONT INPUT

CVNJN1197CFC2
IC20

AVR345(UL) ONLY
AVR345 (EUR) ONLY

option

FROM CONNECT B'D
FROM TUNER MODULE
FROM REG. B'D

** IMPORTANT SAFETY NOTICS.
COMPONENTS IDENTIFIED BY ⚠ MARK HAVE SPECIAL CHARACTERISTICS.
IMPORTANT FOR SAFETY. WHEN REPLACING ANY OF THESE COMPONENTS
USE ONLY MANUFACTURER'S SPECIFIED PARTS.
** THE UNIT OF RESISTANCE IS OHM.
K=1000 OHM , M=1000 KOHM
** THE UNIT OF CAPACITANCE IS MICROFARAD. (uF)
pF=10^{-6} uF
** THIS SCHEMATIC DIAGRAM MAY MODIFIED AT ANY TIME WITH THE
IMPROVEMENT OF PERFORMANCE.

REVISION	2	4	6	
1	3	5	7	

SCHEMATIC DIAGRAM — SHEET

MODEL	AVR254/255/354/355	1/3
DESIGN	CHECK / APPROVE: G.`	DRAWING NO: 2029SCLZ (INPUT) 1/1

CUP12029

HDMI SPDIF MODE : DIR MASTER
HDMI I2S MODE : HDMI MASTER
ADC MODE : DSP MASTER
DIR MODE : DIR MASTER

CRJ10DJ1R0T

<=> HDMI BOARD

*OPTION : EMC COUNTERMEASUER

DATA	CS49700	SDRAM
EXT_D15/SD_D7	29	12
EXT_D14/SD_D6	30	11
EXT_D13/SD_D5	31	9
EXT_D12/SD_D4	32	8
EXT_D11/SD_D3	34	6
EXT_D10/SD_D2	35	5
EXT_D9/SD_D1	37	3
EXT_D8/SD_D0	39	2
EXT_D7/SD_D15	40	49
EXT_D6/SD_D14	41	48
EXT_D5/SD_D13	42	46
EXT_D4/SD_D12	43	45
EXT_D3/SD_D11	45	43
EXT_D2/SD_D10	46	42
EXT_D1/SD_D9	48	40
EXT_D0/SD_D8	49	39

Address	CS49700	SDRAM
EXT_A19	88	
EXT_A18	87	
EXT_A17	85	
EXT_A16	84	
EXT_A15	82	
EXT_A14/SD_A13	77	
EXT_A13/SD_A14	75	19
EXT_A12/SD_A10	74	20
EXT_A11/SD_A12	55	
EXT_A10/SD_A11	56	
EXT_A9/SD_A9	58	32
EXT_A8/SD_A8	59	31
EXT_A7/SD_A7	61	30
EXT_A6/SD_A6	62	29
EXT_A5/SD_A5	64	28
EXT_A4/SD_A4	67	27
EXT_A3/SD_A3	68	24
EXT_A2/SD_A2	70	23
EXT_A1/SD_A1	71	22
EXT_A0/SD_A0	72	21

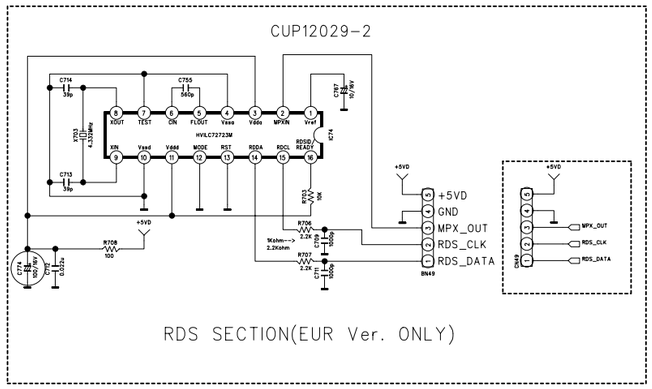
DPP

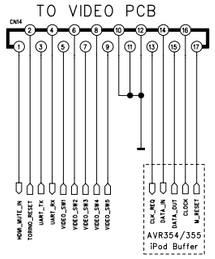
REVISION	2	4	6
1	3	5	7

SCHEMATIC DIAGRAM — SHEET 2/3

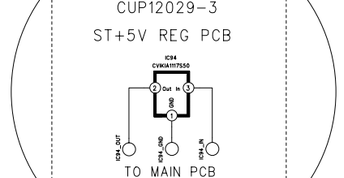
MODEL: AVR254/255/354/355

DESIGN	CHECK	APPROVE	DRAWING NO
			2029SCLZ (DSP) 1/1
18			



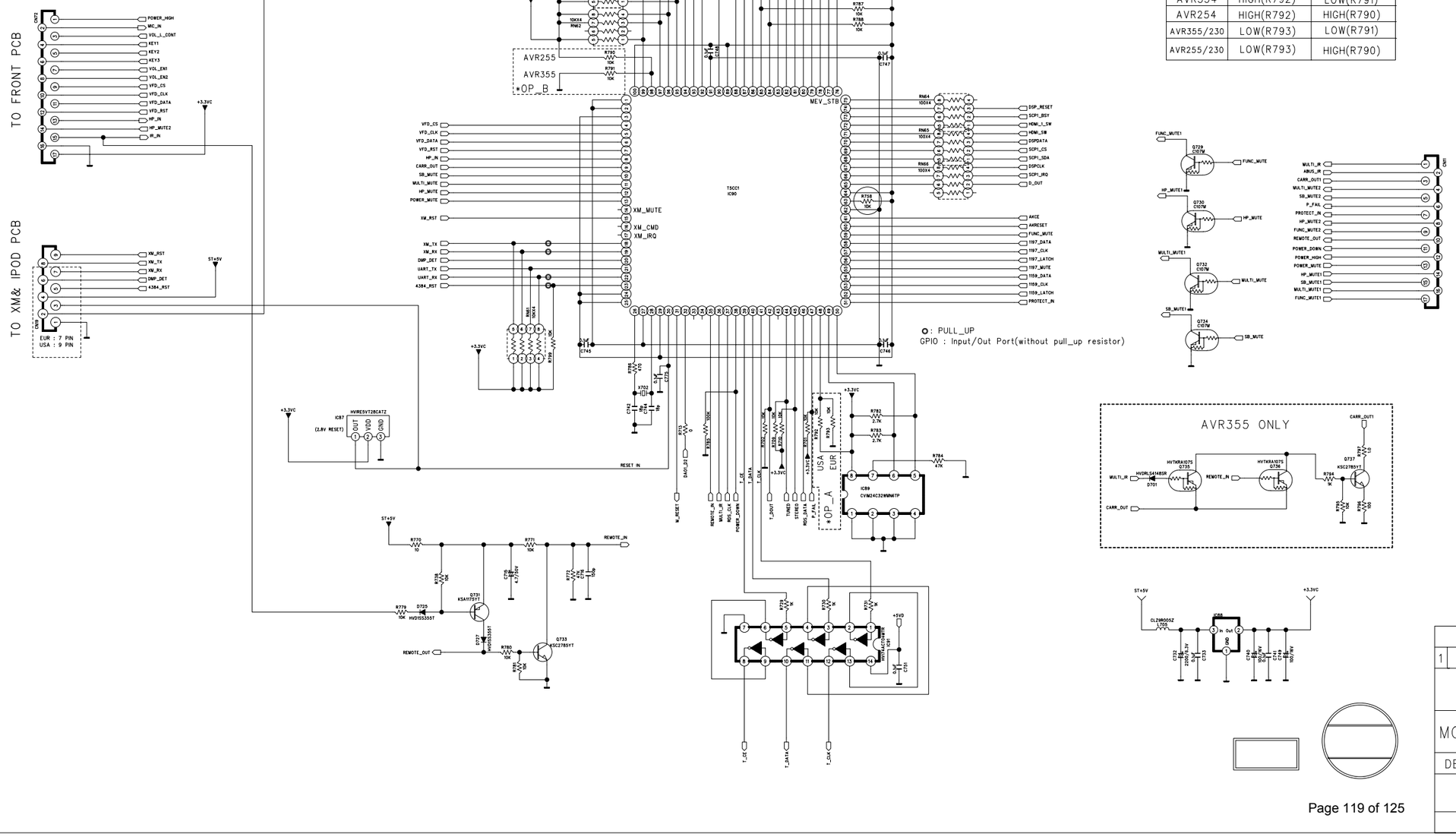


U-COM	AVR255	AVR355	AVR155
PIN 97	HDMI_MUTE_IN	HDMI_MUTE_IN	N.A
PIN 86	TORINO_RESET	TORINO_RESET	N.C
PIN 21	UART_TX(TORNO&PC)	UART_TX(TORNO&PC)	UART_TX(PC)
PIN 22	UART_RX(TORNO&PC)	UART_RX(TORNO&PC)	UART_RX(PC)
PIN 81	VIDEO_SW1	VIDEO_SW1	N.A
PIN 82	VIDEO_SW2	VIDEO_SW2	OSD_CS1
PIN 83	VIDEO_SW3	VIDEO_SW3	OSD_CLK
PIN 84	VIDEO_SW4	VIDEO_SW4	OSD_DA
PIN 85	VIDEO_SW5	VIDEO_SW5	OSD_M
PIN 80		CLOCK	HDMI MUX_SDA
PIN 79		DATA_OUT	HDMI MUX_SCLK
PIN 77		DATA_IN	OSD_H
PIN 76		CLK-REQ	



* MODEL OPTION *

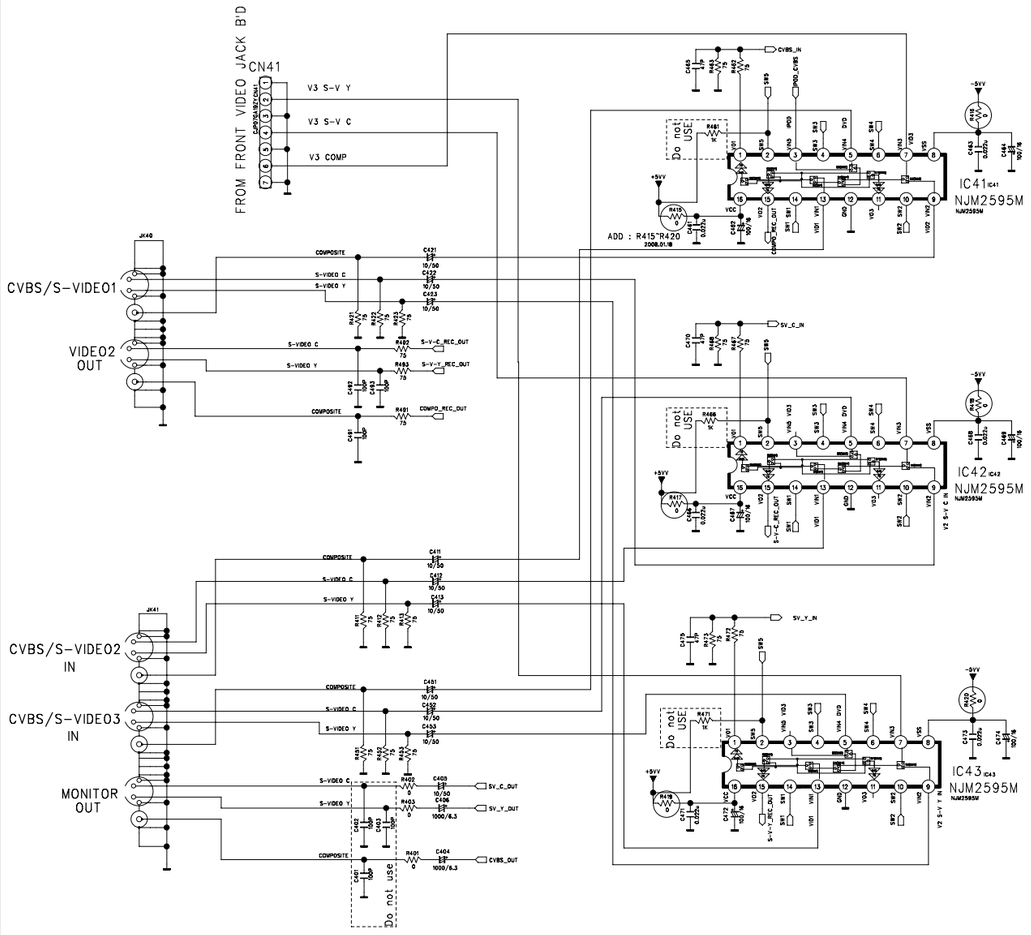
MODEL	OP_A(PIN48)	OP_B(PIN98)
AVR355	HIGH(R792)	LOW(R791)
AVR354	HIGH(R792)	LOW(R791)
AVR254	HIGH(R792)	HIGH(R790)
AVR355/230	LOW(R793)	LOW(R791)
AVR255/230	LOW(R793)	HIGH(R790)

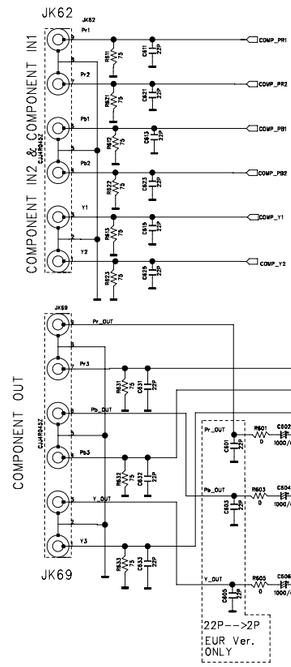


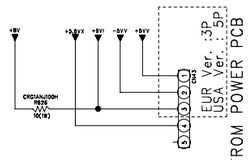
REVISION	2	4	6	
1	3	5	7	

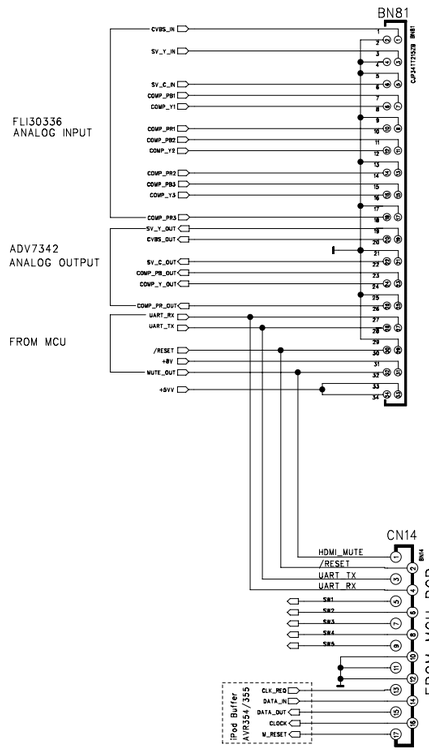
SCHEMATIC DIAGRAM			SHEET
MODEL	AVR254/255/354/355		3/3
DESIGN	CHECK	APPROVE	DRAWING NO
		G.S	2029SCLZ (CPU) 1/1

CUP12033Z









* DEFINITION OF I2C REGISTER (NJW1321)

I2C BUS FORMAT

MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB
S(1BIT)	SLAVE ADDRESS(8BIT)	A(1BIT)	DATA(8BIT)	A(1BIT)	DATA(8BIT)	A(1BIT)	P(1BIT)

S : Starting Term
A : Acknowledge Bit
P : Ending Term

SLAVE ADDRESS

MSB	Slave Address(8BIT)							MSB	Hex
1	0	0	0	0	0	ADR(1BIT)		R/NOT W(1BIT)	--

R/NOT W : Set the Write Mode or Read Mode.
ADR : Set the Slave Address by " ADR" terminal.
R/NOT W = 0 : WRITE MODE, ADR = 0/1 ; ADR=0 Hex94(h), ADR=1 Hex96(h)
R/NOT W = 0 : READ MODE, ADR = 0/1 ; ADR=0 Hex95(h), ADR=1 Hex97(h)

CONTROL REGISTER TABLE

<WRITE MODE>

NO.	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
DATA 1	PS1	PS2	OUT1			OUT2		
DATA 2	AUX0		AUX1		AUX2		AUX3	

PS : POWER SAVE
=> PS = 1 ; POWER SAVE ON (MUTE), PS = 0 ; POWER SAVE OFF (OUT ON)
OUT : OUTPUT
AUX : AUXILIARY (CONTROL SIGNAL OUTPUT)

<READ MODE>

NO.	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
DATA	PORT0		PORT1		PORT2		PORT3	

PORT : INPUT

*NJM2595M OPTION
==>V_MUTE "LOW" ACTIVE

FUNC.	SW1	SW2	SW3	SW4	SW5
CVBS/S-V1	H	L	L	L	H
CVBS/S-V2	L	H	L	L	H
CVBS/S-V3	H	L	L	H	H
FRONT CVBS/S-V	H	H	L	L	H
IPOD	H	L	H	H	H

* AVR345
*NO.4

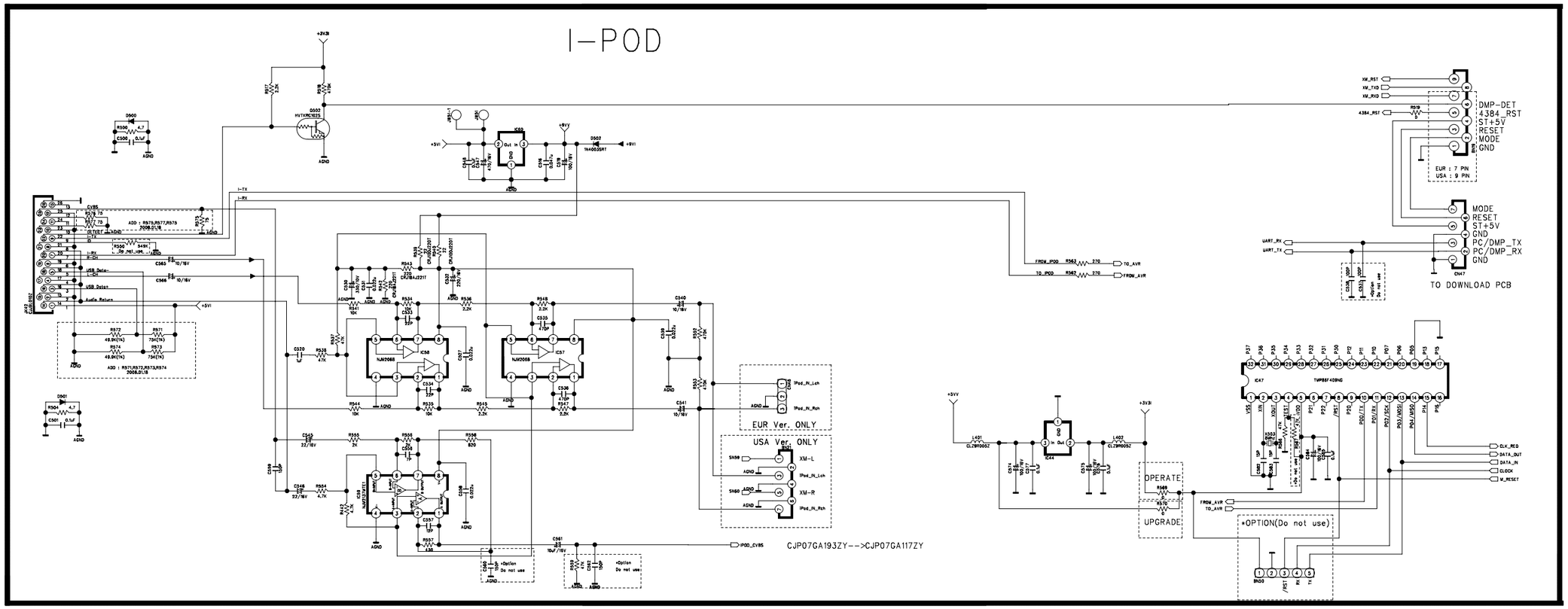
REVISION	2		4		6	
1		3		5		7

SCHEMATIC DIAGRAM — SHEET 1/2

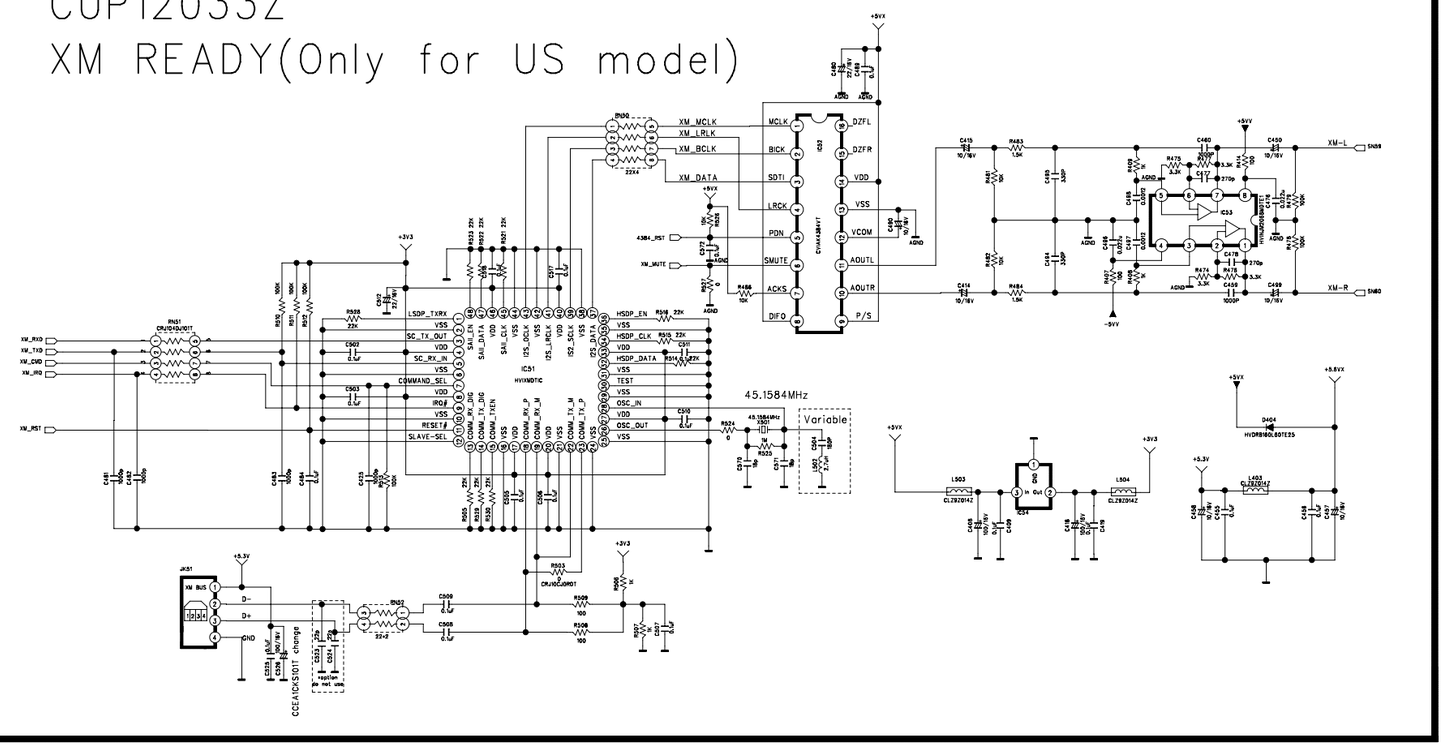
MODEL	AVR354 /355	
DESIGN	CHECK	APPROVE
		DRAWING NO
		2033SCEZ
06.08.23	06.	06.
		(VIDEO) 1/1

DPP

I-POD



CUP12033Z
XM READY(Only for US model)



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REVISION	2	4	6
1	3	5	7

SCHEMATIC DIAGRAM — SHEET 1/4

MODEL	AVR354 / 355	
DESIGN	CHECK	APPROVE	DRAWING NO
05.00.00	05.00.00	05.00.00	2033SCEZ (AMP) 1/1

SR-CH

BL-CH

SL-CH

EXCEPT AVR154/155

BR-CH

C-CH

FR-CH

FL-CH

2SD2389P:AVR154
2SD2390:AVR155/254/255
2SD2560:AVR354/355

2SB1559P:AVR154
2SB1560:AVR155/254/255
2SB1647:AVR354/355

GAIN	R561, R562, R563, R564, R565, R850 R851
AVR154/155	1.8K
AVR255/355	1.6K

AVR354/355 ONLY

JW90,JW91 : ALL MODELS

DC PROTECTOR

THERMAL PROTECTOR

OVERLOAD DETECTION

FAN

ONLY FAN USING

JW92: AVR154/155 ONLY

JK91

JK92

BN19

BN20

EXCEPT AVR154/155

ONLY AVR154/155

FOR USING FAN

AVR254/255/354/355 PART

TO REMOTE IN/OUT B'D

FROM TRANS

AC IN

CJA5238Y4 (USA) : AVR154/155/254/255
CJA2044ZA (EUR) : AVR154/230,155/220,234/230,255/230
AVR354,355,354/230,355/230 : CR2R4001BN01A, CJA5006ZW
CJA2417BZ (USA) : AVR354/355
CJA2805AZ (EUR) : AVR354/230, 355/230

JW93, OL91, F902 : EXCEPT AVR154

FROM INPUT B'D

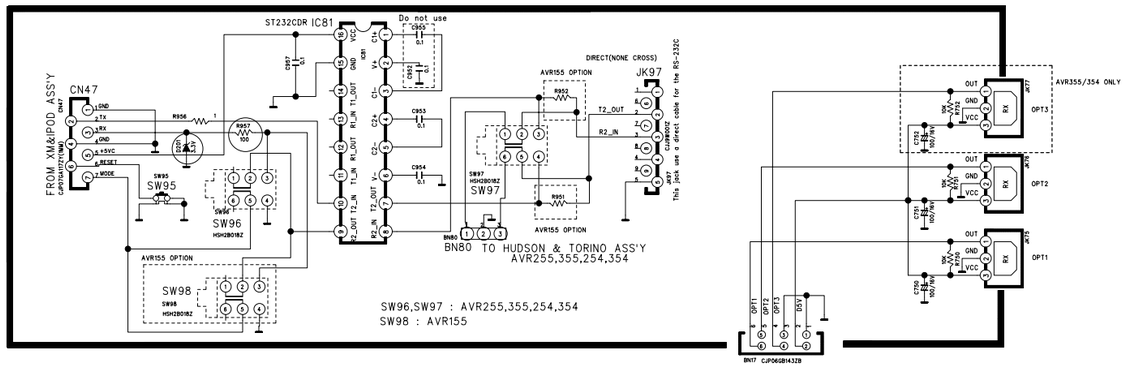
FROM TRANS B'D

AVR254/255/354/355 OPTION

** IMPORTNAT SAFETY NOTICE.
IMPORTANT FOR SAFETY WHEN REPLACING ANY OF THESE COMPONENTS
USE ONLY MANUFACTURE'S SPECIFIED PARTS.
** THE UNIT OF RESISTANCE IS OHM.
K=1000 OHM, M=1000 KOHM.
** THE UNIT OF CAPACITANCE IS MICROFARAD (uF)
pF = 10^-6 uF
** THIS SCHEMATIC DIAGRAM MAY MODIFIED AT ANY TIME WIHE THE
IMPROVEMENT OF PERFORMANCE

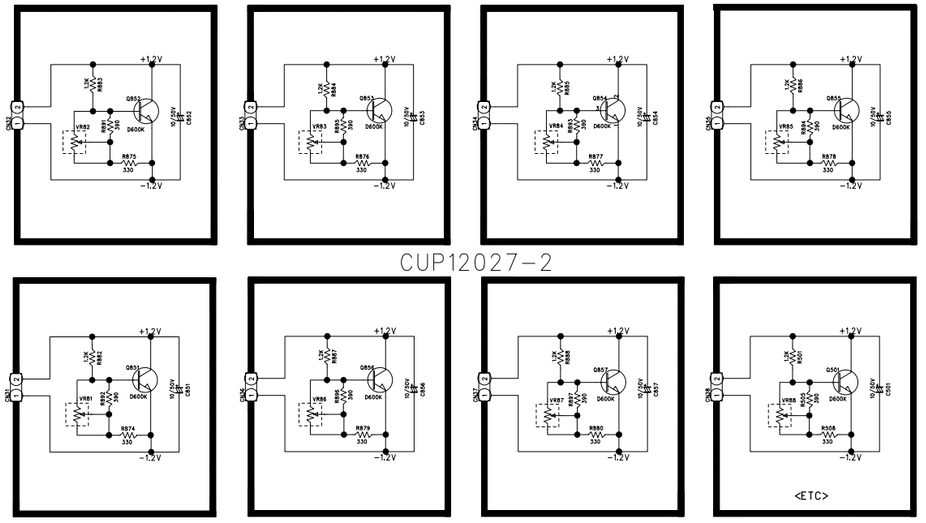
REVISION	1	2	3	SHEET
SCHEMATIC DIAGRAM				
MODEL	AVR154/155/254/255/354/355			2 / 7
DESIGN	CHECK	APPROVE	Γ	
			(MAIN)	1/1
23				

CUP12027-1

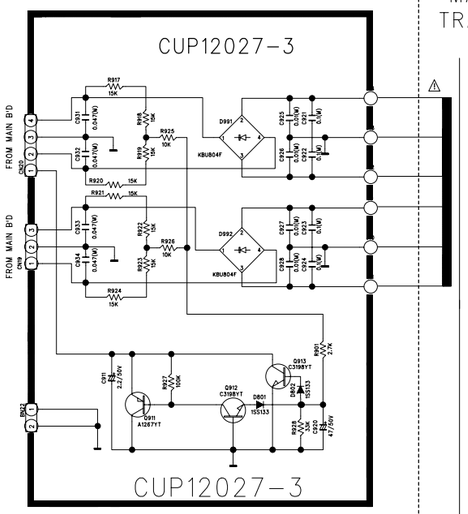


< OPTICAL IN & RS-232 PCB >

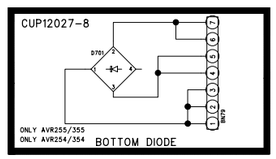
< BIAS T.R PCB >



CUP12027-3

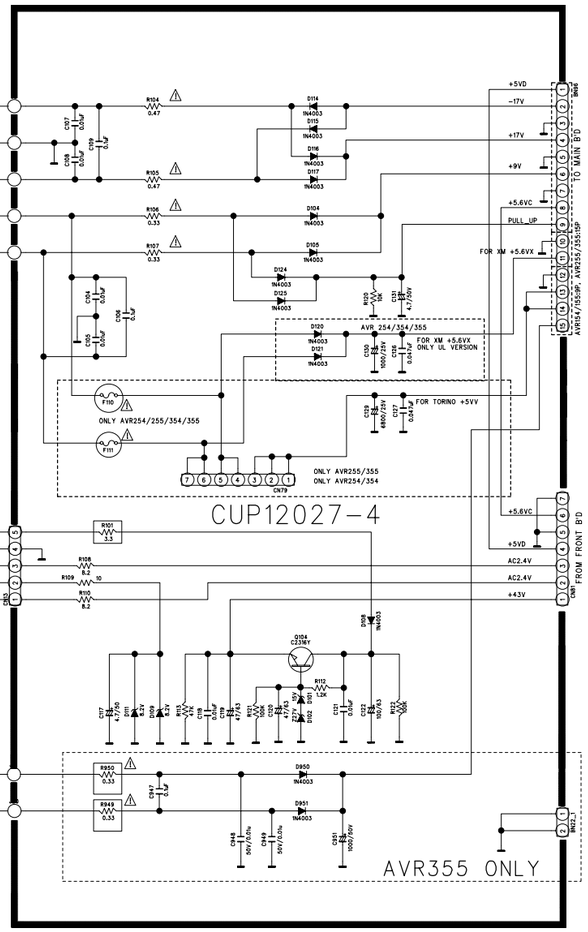


CUP12027-8

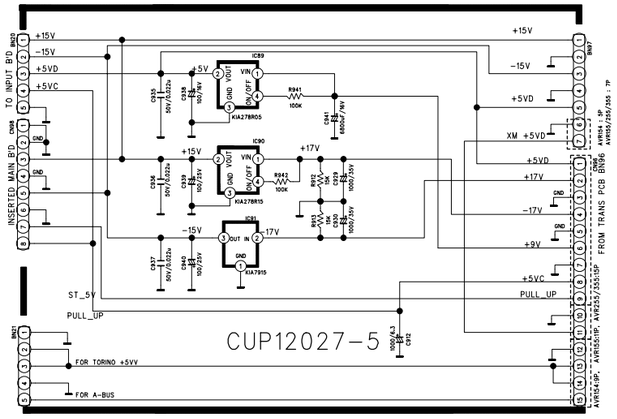


USA : AC120V 60Hz
EUR : AC230V 50Hz

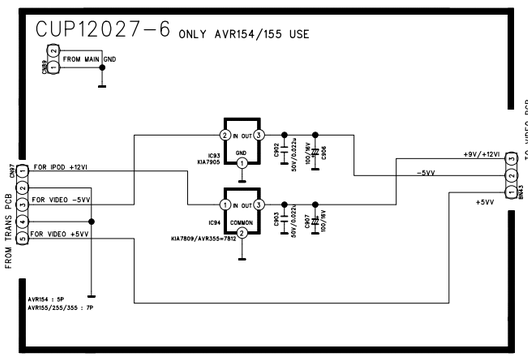
MAIN TRANS



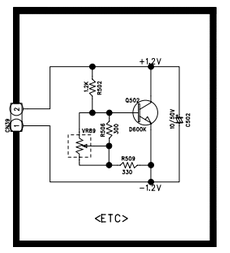
< TRANS PCB >

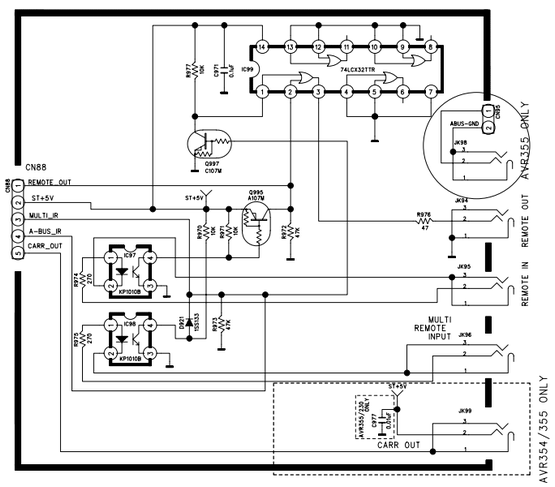


CUP12027-6 ONLY AVR154/155 USE



< REGULATOR PCB >





AVR254/255/354/355 ONLY CUP12027-7

< REMOTE IN/OUT PCB >

M P

SUE

REVISION	2	4	
1	3		

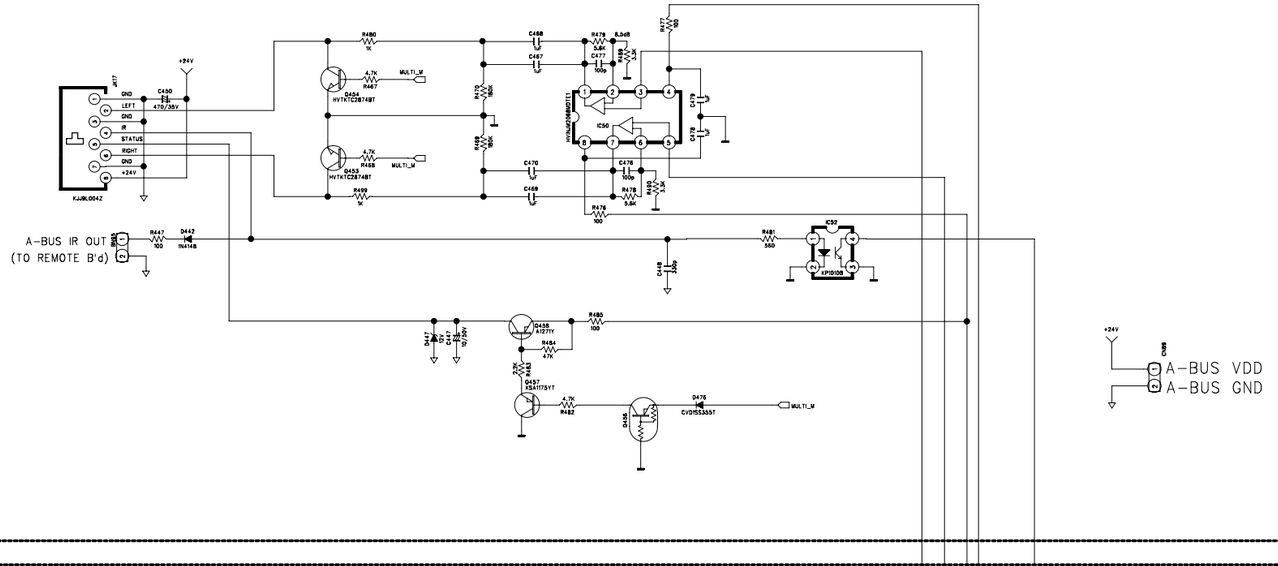
SCHEMATIC DIAGRAM — SHEET

MODEL	AVR x54/x55	1/1

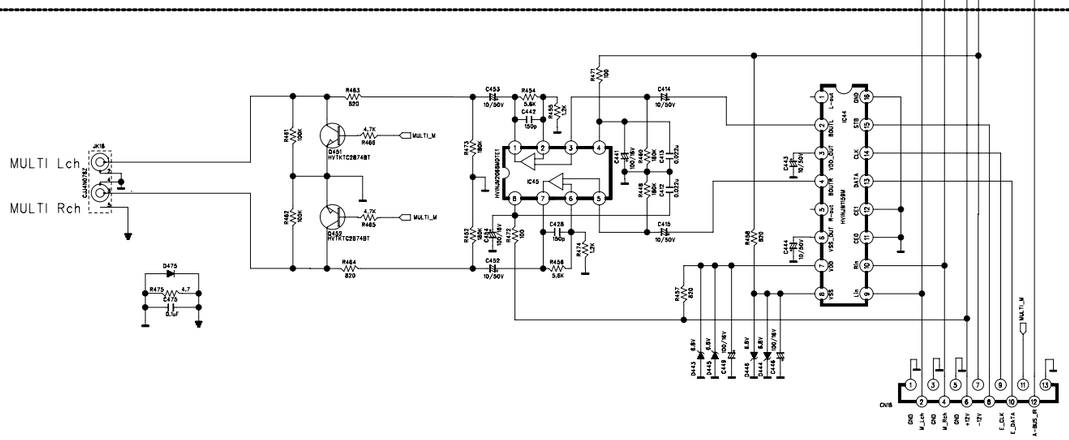
DESIGN	CHECK	APPROVE	DRAWING NO
			CUP12027Z (POWER) 1/1

CUP12036Z

A-BUS PART : ONLY FOR AVR355 & AVR355/230



MULTI ROOM VOLUME : AVR355, AVR354, AVR355/230



E/S

8.08

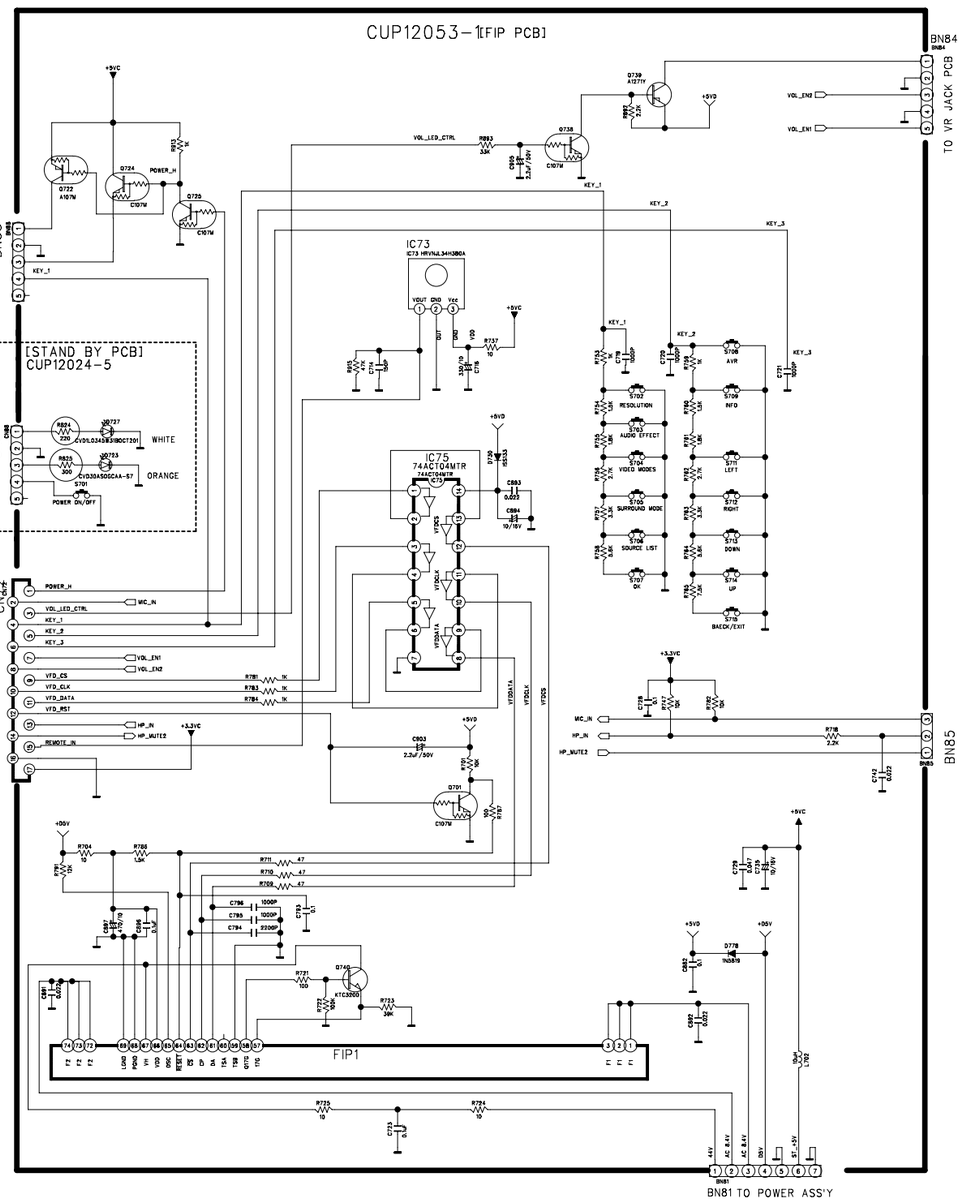
REVISION	2		4		6	
1		3		5		7	

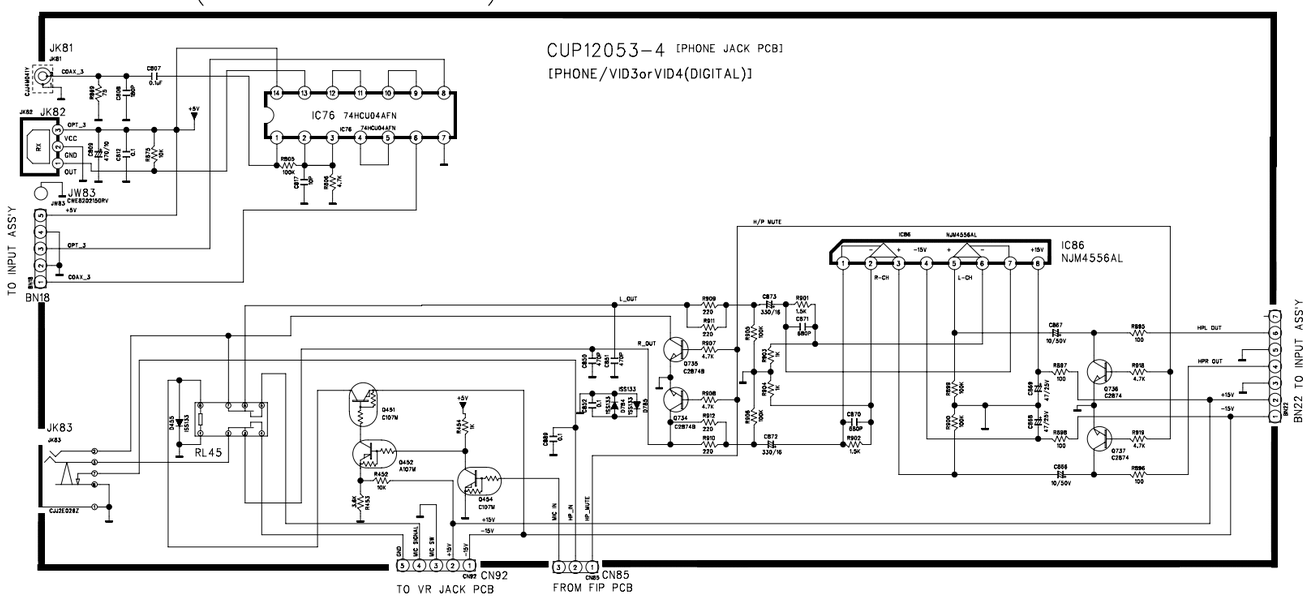
SCHEMATIC DIAGRAM — SHEET

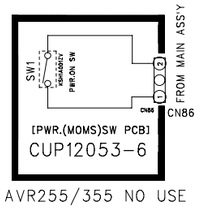
MODEL: AVR354/355

DESIGN	CHECK	APPROVE	DRAWING NO
		G.	
07.10.18			

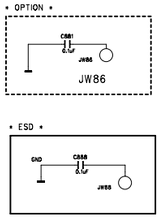
AVR 255/355 FRONT (CUP12053Z)

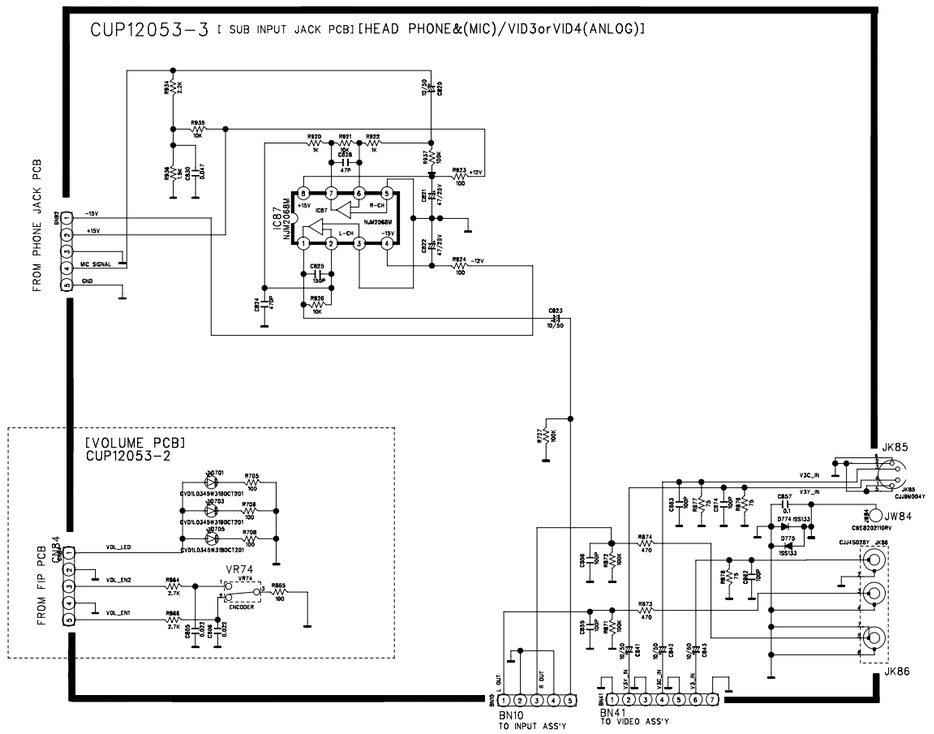






AVR255/355 NO USE





REVISION	2				
1					

SCHEMATIC DIAGRAM			SHEET 1/7
MODEL	AVR255/355		
DESIGN	CHECK	APPROVE	DRAWING NO
05			CUP12053Z (FRONT) 1/1

MULTI. LAY 2008. 1.15